Introduction to FPGA

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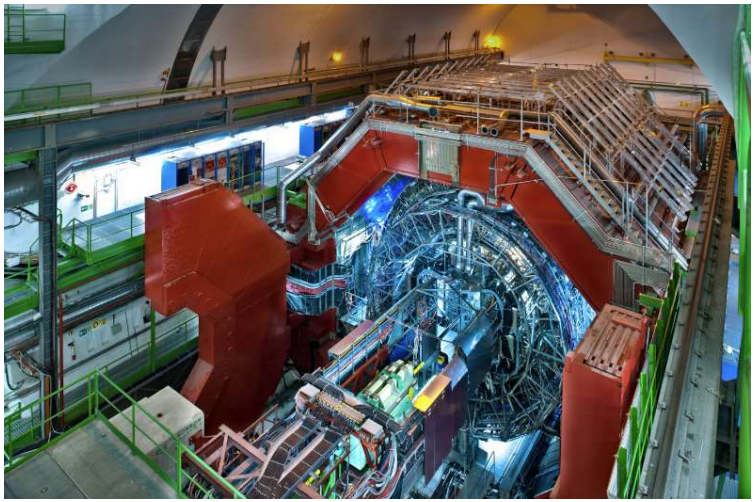
Lectures on Modern Scientific Programing 2022 14 November 2022

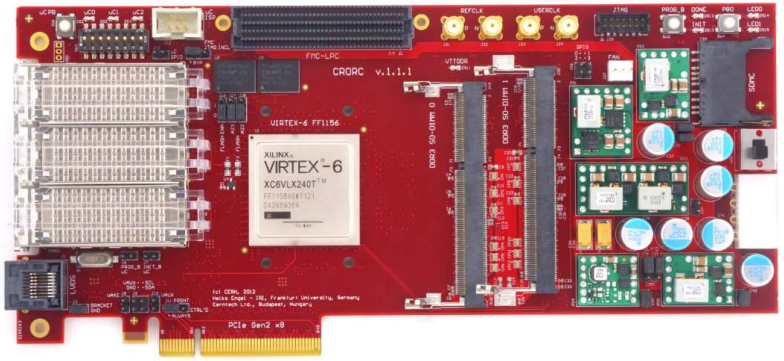
CERN ALICE Experiment

- LHC Run 3 (2022 – 2026)
- CRU (Common Readout Unit)
- 48 x 4.8 Gb/s Optical links
- Wigner RPC (HW prod., FW dev.)

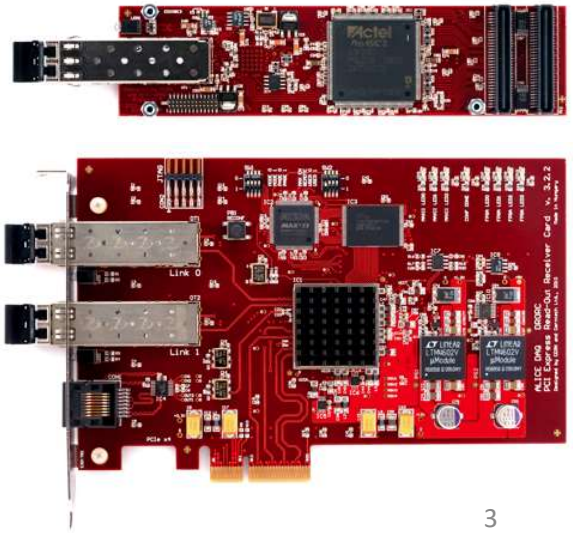


CERN ALICE Experiment

- LHC Run2 (2015 – 2019)
- C-RORC
- 12 x 4 Gb/s Optical links

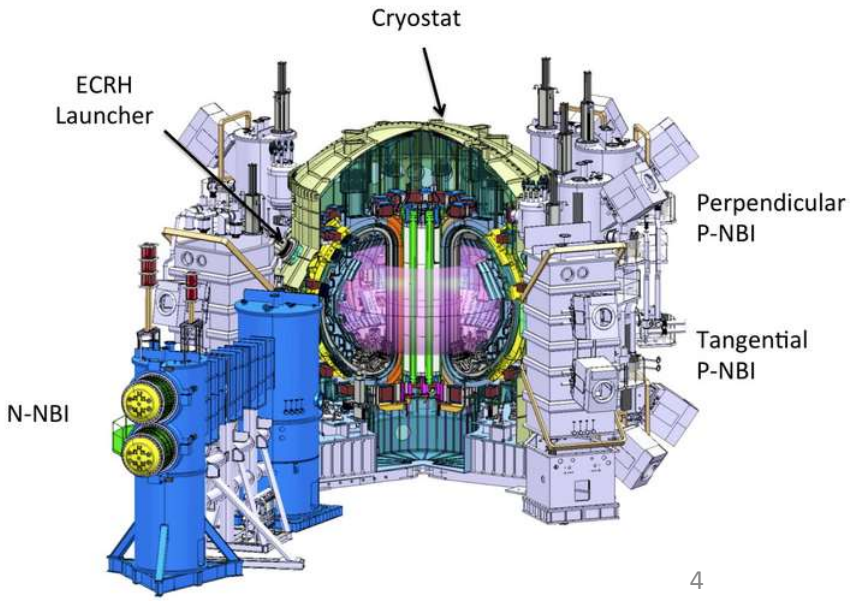


- LHC Run 1 (2009 - 2013)
- SIU + RORC
- 2 x 2 Gb/s Optical links
- Developed by Wigner RCP



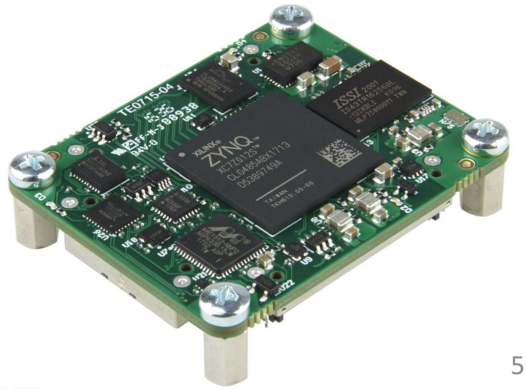
Wigner EDICAM

- EDICAM (Event Detection Intelligent Camera)
- HS (10Gb/s) camera for plasma monitoring
- Used in:
  - Germany (Wendelstein 7-X exp.)
  - Japan (JT-60SA exp.)
- Developed by Wigner RCP and Cerntech Ltd



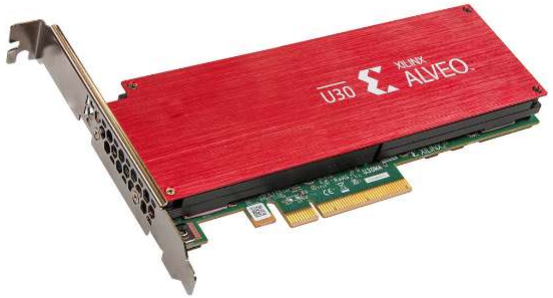
Lombiq Hastlayer

- FPGA based .NET accelerator framework
- Variants:
  - Cloud based – MS Azure with Alveo U250
  - Standalone – embedded applications
- FPGA layer developed by Wigner RCP



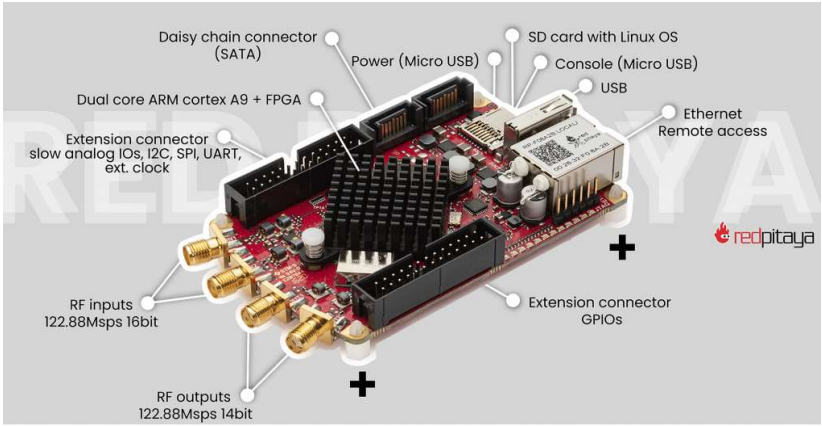
Amazon EC2 F1 and VT1

- Amazon EC2 F1 instances use FPGAs to enable delivery of custom hardware accelerations. Examples of target applications that can benefit from F1 instance acceleration are genomics, search/analytics, image and video processing, network security, electronic design automation (EDA), image and file compression and big data analytics.
- Amazon EC2 VT1 instances are designed to accelerate real time video transcoding and deliver low cost transcoding for live video streams.



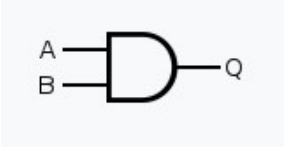
SDR (Software Defined Radio)

- Red Pitaya SDRlab 122-16 kit:
- 2 x 122.88MS/s 16-bit ADC
- Software-defined radio
- RF HF applications
- Space and military RF applications
- FFT analysis and signal measurement
- Environmental electromagnetic measurements
- Universal test platform for RF prototyping



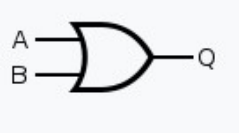
Inside the FPGA – AND, OR, NOT gates

- AND



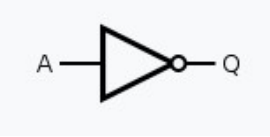
INPUT		OUTPUT
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

- OR



INPUT		OUTPUT
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

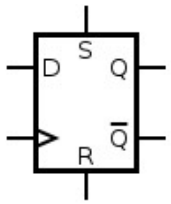
- NOT



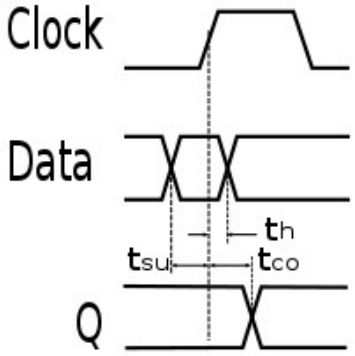
INPUT	OUTPUT
A	Q
0	1
1	0

Inside the FPGA – D flip-flop

- D flip-flop



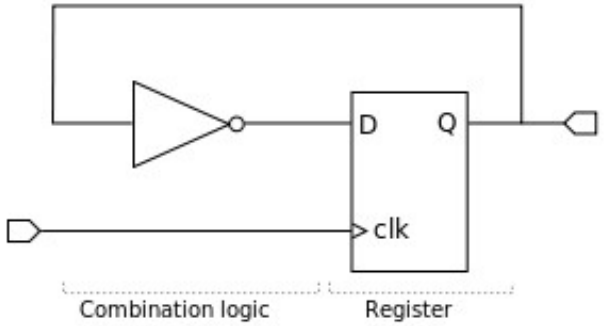
Clock	D	Q_{next}
Rising edge	0	0
Rising edge	1	1
Non-rising	X	Q

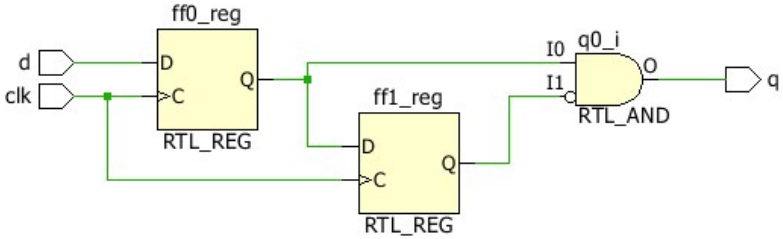


Inputs				Outputs	
S	R	D	>	Q	$\overline{Q}$
0	1	X	X	0	1
1	0	X	X	1	0
1	1	X	X	1	1

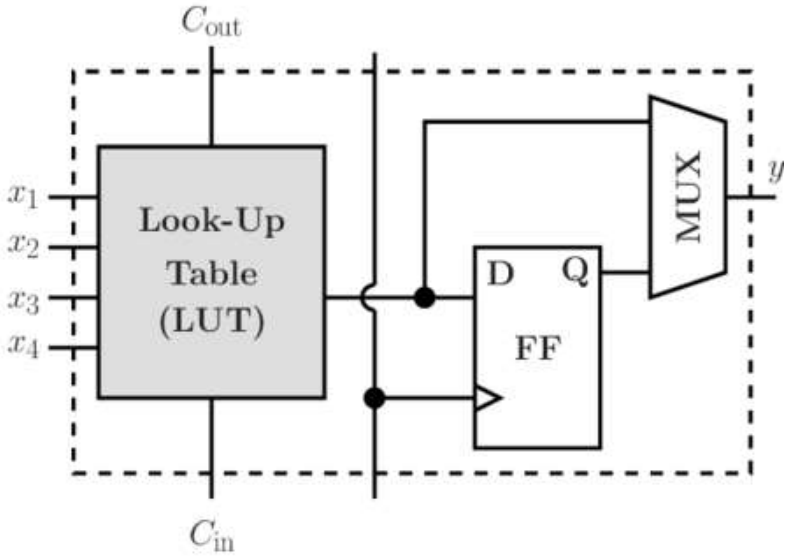
Inside the FPGA – RTL

- Register-transfer level (RTL)
- Snchronous circuit:
  - registers (sequential logic)
  - combinational logic
- Fmax depends on the longest combinational logic path

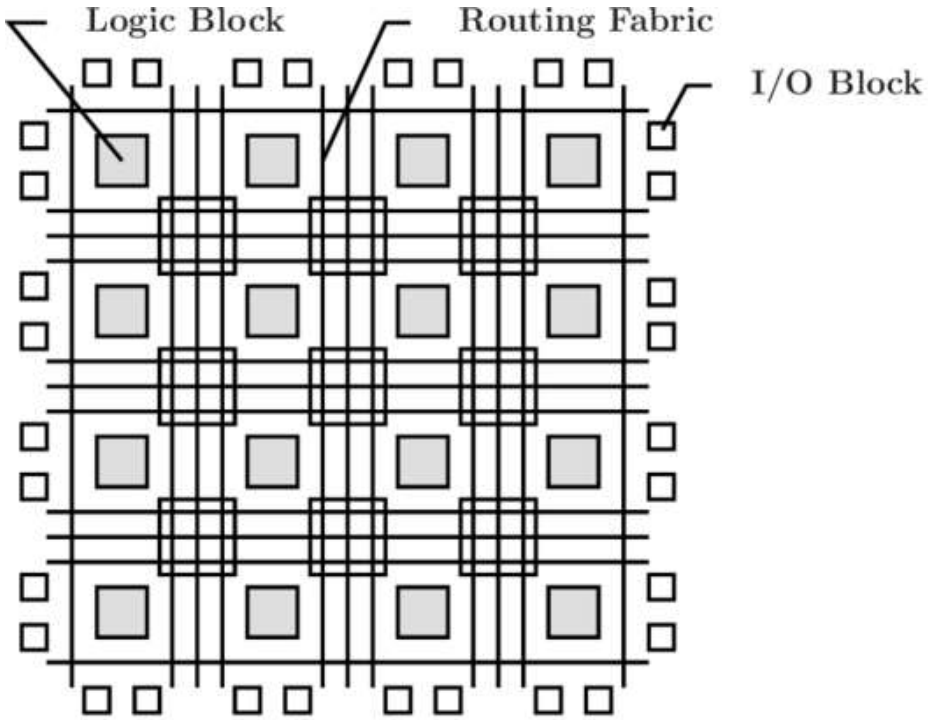




Inside the FPGA - Fabric



Logic Block



FPGA Fabric

Source: ResearchGate

Inside the FPGA - Memory, MGT, CPU

- Memory:
  - Internal: BRAM
  - External: SRAM, FLASH, DDR, HBM
- Multi gigabit transceiver:
  - 1 Gbps to 56 Gbps
- CPU:
  - Softcore: Nios, MicroBlaze, RISC
  - Hardcore: single/dual core 32/64-bit ARM

FPGA Vendors - Xilinx / AMD

SPARTAN SPARTAN 7 ARTIX 7 ARTIX UltraSCALE+ ZYNQ ZYNQ UltraSCALE+ CoolRunner-II

AMD XILINX

Zynq® UltraScale+™ MPSoCs

		Device Name[1]	ZU1CG/EG	ZU2CG/EG	ZU3CG/EG	ZU3TCG/EG	ZU4CG/EG	ZU5CG/EG	ZU6CG/EG	ZU7CG/EG	ZU9CG/EG
Processing System (PS)	Application Processor Unit	Processor Core	**Dual-core/Quad-core** Arm® Cortex®-A53 MPCore™ up to 1.3GHz								
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB								
	Real-Time Processor Unit	Processor Core	**Dual-core** Arm Cortex-R5F MPCore up to 533MHz								
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core								
	External Memory	Dynamic Memory Interface	x16: DDR4 w/o ECC; x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 w/ ECC								
		Static Memory Interfaces	NAND, 2x Quad-SPI								
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet								
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO								
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains								
		Security	RSA, AES, and SHA								
		AMS - System Monitor	10-bit, 1MSPS – Temperature and Voltage Monitor								
PS to PL Interface			12 x 32/64/128b AXI Ports								
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	81	103	154	157	192	256	469	504	600
		CLB Flip-Flops (K)	74	94	141	144	176	234	429	461	548
		CLB LUTs (K)	37	47	71	72	88	117	215	230	274
	Memory	Distributed RAM (Mb)	1.0	1.2	1.8	2.1	2.6	3.5	6.9	6.2	8.8
		Total Block RAM (Mb)	3.8	5.3	7.6	5.1	4.5	5.1	25.1	11.0	32.1
		UltraRAM (Mb)	-	-	-	14.0	13.5	18.0	-	27.0	-
	Clocking	Clock Management Tiles (CMTs)	3	3	3	1	4	4	4	8	4
	Integrated IP	DSP Slices	216	240	360	576	728	1,248	1,973	1,728	2,520
		PCI Express®	-	-	-	1x Gen3x8	2x Gen3x8[2]	2x Gen3x8[2]	-	1x Gen3x16 & 1x Gen3x8	-
		150G Interlaken	-	-	-	-	-	-	-	-	-
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-	-	-	-	-	-
		AMS - System Monitor	2	2	2	2	2	2	2	2	2
	Transceivers	GTH Transceivers[3]	-	-	-	8	16	16	24	24	24
		GTY Transceivers	-	-	-	-	-	-	-	-	-
	Speed Grades	Extended[4]	-1 -2 -2L				-1 -2 -2L -3				
		Industrial	-1 -1L -2								

Xilinx Alveo Product Lineup

ALVEO. U50	ALVEO. U200	ALVEO. U250	ALVEO. U280
			
UltraScale+ Architecture	UltraScale+ Architecture	UltraScale+ Architecture	UltraScale+ Architecture
872k LUTs	1,182k LUTs	1,728k LUTs	1,304k LUTs
Single slot, half height	Dual slot, full height	Dual slot, full height	Dual slot, full height
8GB HBM2, 460GB/sec	64GB DDR, 77GB/sec	64GB DDR, 77GB/sec	8GB HBM2, 460GB/sec
PCIe Gen3, Gen4, CCIX	PCIe Gen3	PCIe Gen3	PCIe Gen3, Gen4, CCIX
1x QSFP 28 (100GbE)	2x QSFP 28 (100GbE)	2x QSFP 28 (100GbE)	2x QSFP 28 (100GbE)
< 75W	< 225W	< 225W	< 225W

Source: Xilinx

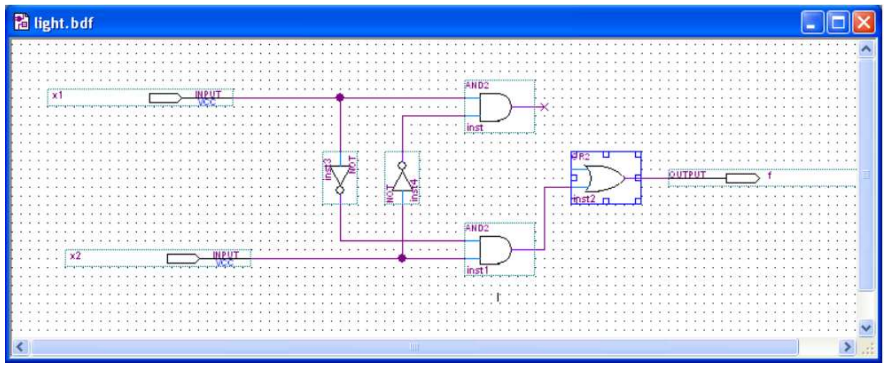
FPGA Vendors - Altera / Intel

- Cyclone, Arria, Stratix, Agilex

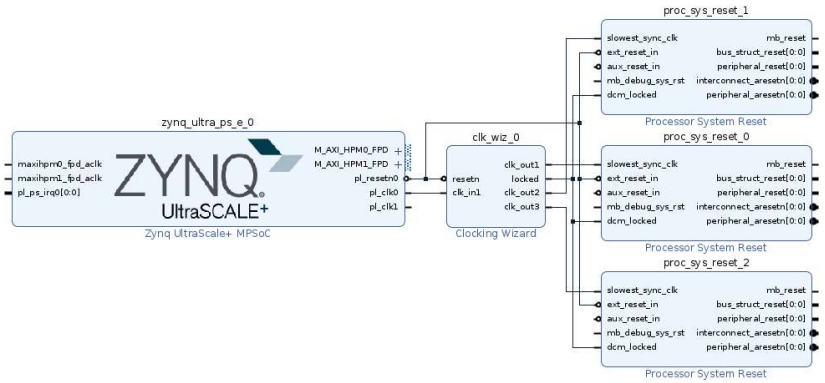
	PRODUCT LINE	AGF 006	AGF 008	AGF 012	AGF 014	AGF 019	AGF 022	AGF 023	AGF 027
Resources	Logic elements (LEs)	573,480	764,640	1,178,525	1,437,240	1,918,975	2,208,075	2,308,080	2,692,760
	Adaptive logic modules (ALMs)	194,400	259,200	399,500	487,200	650,500	748,500	782,400	912,800
	ALM registers	777,600	1,036,800	1,598,000	1,948,800	2,602,000	2,994,000	3,129,600	3,651,200
	High-performance crypto blocks	0	0	0	0	2	0	2	0
	eSRAM memory blocks	0	0	2	2	1	0	1	0
	eSRAM memory size (Mb)	0	0	36	36	18	0	18	0
	M20K memory blocks	2,844	3,792	5,900	7,110	8,500	10,900	10,464	13,272
	M20K memory size (Mb)	56	74	115	139	166	212	204	259
	MLAB memory count	9,720	12,960	19,975	24,360	32,525	37,425	39,120	45,640
	MLAB memory size (Mb)	6	8	12	15	20	23	24	28
	I/O PLL	12	12	16	16	10	16	10	16
	Variable-precision digital signal processing (DSP) blocks	1,640	2,296	3,743	4,510	1,354	6,250	1,640	8,528
	18 x 19 multipliers	3,280	4,592	7,486	9,020	2,708	12,500	3,280	17,056
	Single-precision or half-precision tera floating point operations per second (TFLOPS)	2.5 / 5.0	3.5 / 6.9	6.0 / 12.0	6.8 / 13.6	2.0 / 4.0	9.4 / 18.8	2.5 / 5.0	12.8 / 25.6
	Maximum EMIF x72	2	2	4	4	2	4	2	4

FPGA programming - Schematic

- Same schematic as for discrete parts
- It is still viable for simpler designs



- Still used as top level module
- To visually integrate different Ips and HDL modules



FPGA programming - Verilog

- First appeared in 1984
- C like syntax
- Weakly typed
- Easier to begin with
- Verilog-95, Verilog-2001, SystemVerilog

```
module toplevel(clock,reset);
  input clock;
  input reset;

  reg flop1;
  reg flop2;

  always @ (posedge reset or posedge clock)
    if (reset)
      begin
        flop1 <= 0;
        flop2 <= 1;
      end
    else
      begin
        flop1 <= flop2;
        flop2 <= flop1;
      end
endmodule
```

FPGA programming - VHDL

- First appeared in 1980s
- VHSIC Hardware Description Language (VHDL)
- Very High-Speed Integrated Circuits Program (VHSIC)
- ADA/Pascal like syntax
- Strongly typed

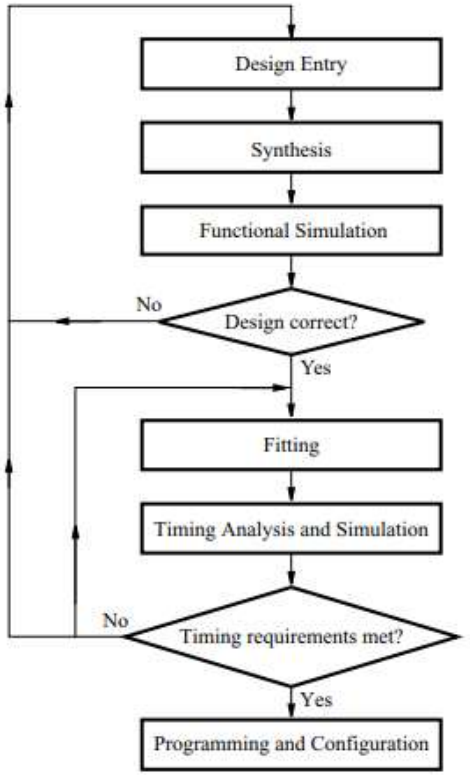
```
library IEEE;
use IEEE.std_logic_1164.all;

-- this is the entity
entity ANDGATE is
  port (
    I1 : in std_logic;
    I2 : in std_logic;
    O  : out std_logic);
end entity ANDGATE;

-- this is the architecture
architecture RTL of ANDGATE is
begin
  O <= I1 and I2;
end architecture RTL;
```

FPGA programming – High Level Synthesis

- Aim: Reuse the existing algorithms written in high level languages
- Problems:
  - No timing information
  - How to control parallelism
- Examples:
  - Catapult C / Impulse C / SystemC
  - OpenCL – supported by both Xilinx and Altera
  - Hastlayer - .NET assembly to VHDL conversion
  - MaxCompiler - Converts dataflow computing systems to RTL

Typical FPGA design flow

- Source codes: schematic, Verilog, VHDL
- Synthesis: RTL (Register Transfer Level)
- Simulation: ISIM, ModelSim
- Mapping: RTL to fabric
- Routing
- Static timing analysis
- Debugging: ChipScope, SignalTap

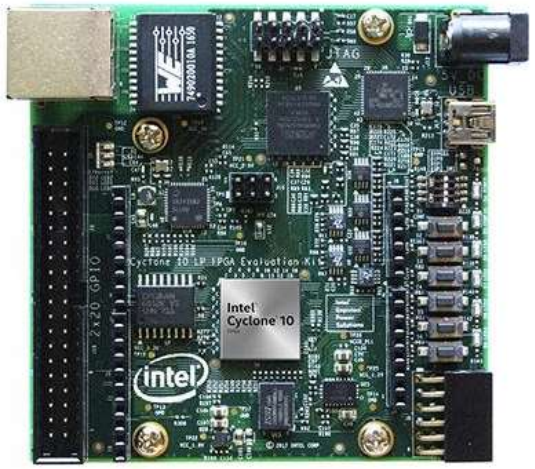


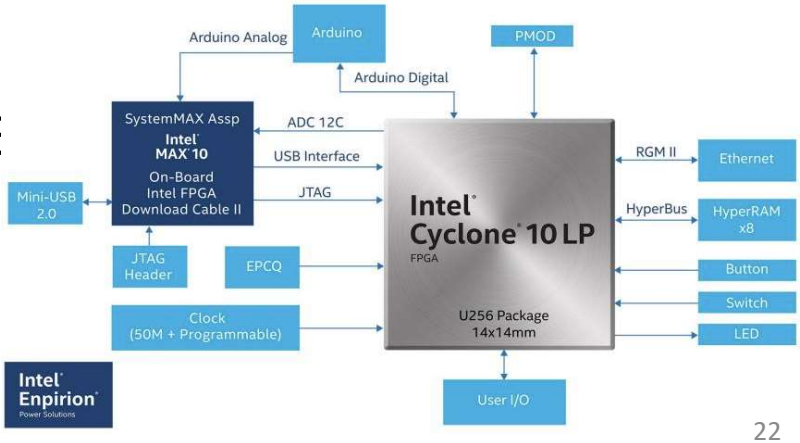
DIY - fpga4fun.com

- Multiple small fun projects (Verilog)
- Interfaces: I2C, SPI, SD card, PCI Express, Ethernet, HDMI, ...
- Basic projects: music box, LED displays, Pong game, ...
- Advanced projects: Digital oscilloscope, Graphic LCD panel, CNC steppers, Spoc CPU core, …

DIY - Intel Cyclone 10 LP Evaluation Board

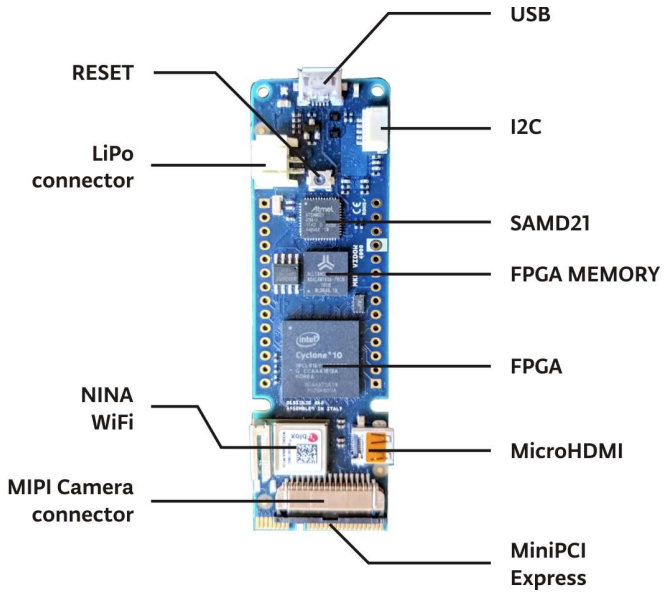
- Intel Cyclone 10 LP (10CL025U256 25K LE)
- 128 Mb HyperRAM Memory
- 10/100/1000Mbps Ethernet Interface
- Arduino header to accept UNO R3 compatible Shields
- Digilent Pmod Connector
- General-purpose through-hole connector
- Switch, push buttons, jumpers, and status LE
- Powered by USB or via 5V dc input
- 99.95 USD





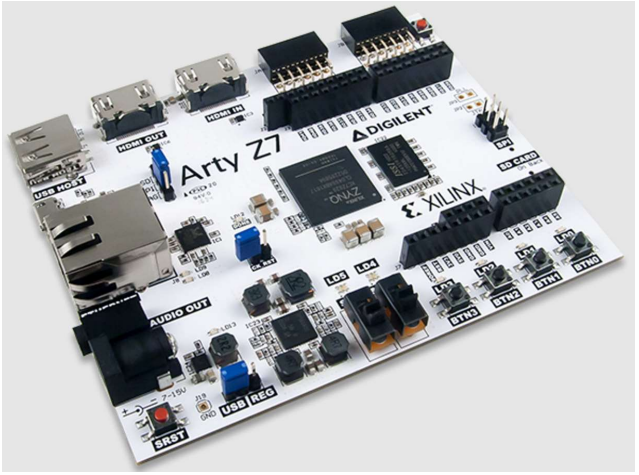
DIY - Arduino MKR Vidor 4000

- SAMD21 Cortex®-M0+ 32bit low power ARM MC
- u-blox NINA-W102 (Wi-Fi + Bluetooth)
- Intel Cyclone 10CL016 FPGA
- MIPI camera connector
- 22 I/O pins + 25 Mini PCI Express pins
- Flash 2 MB
- SDRAM 8 MB
- Micro HDMI output
- 75 EUR



DIY - Digilent Arty Z7 SoC Development Board

- Zynq-7010 SoC FPGA
- Dual-core Cortex-A9 650MHz processor
- DDR3 memory controller
- 512MB DDR3 @ 1050Mbps
- 16MB Quad-SPI Flash
- Gigabit Ethernet PHY
- Two standard Pmod ports
- 16 Total FPGA I/O
- Arduino Shield connector
- push-buttons, switches, LEDs



Thank You
For Your Attention!

Any Questions?