Implementing CERN GBT and lpGBT link arrays in Intel Arria 10 FPGA

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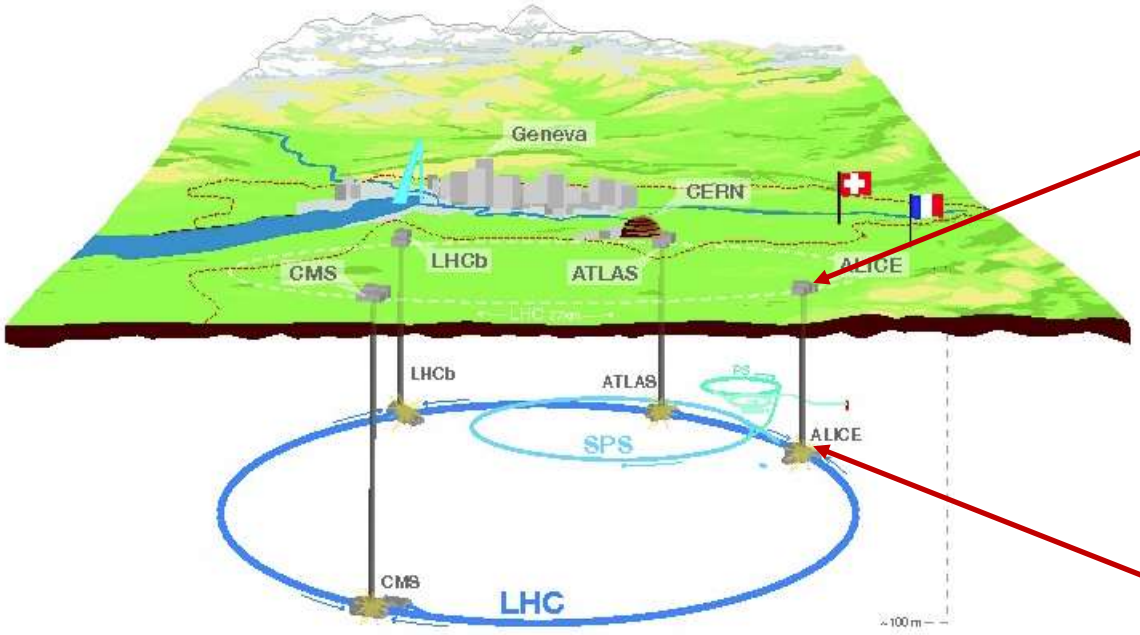
GPU Day 2023 16 May 2023

CERN Large Hadron Collider (LHC)

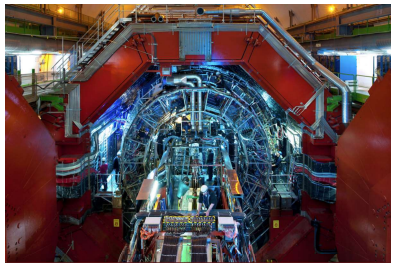


Ref: CERN

Counting room

Down link:
LHC clock,
trigger,
slow control

Up link:
Detector
data



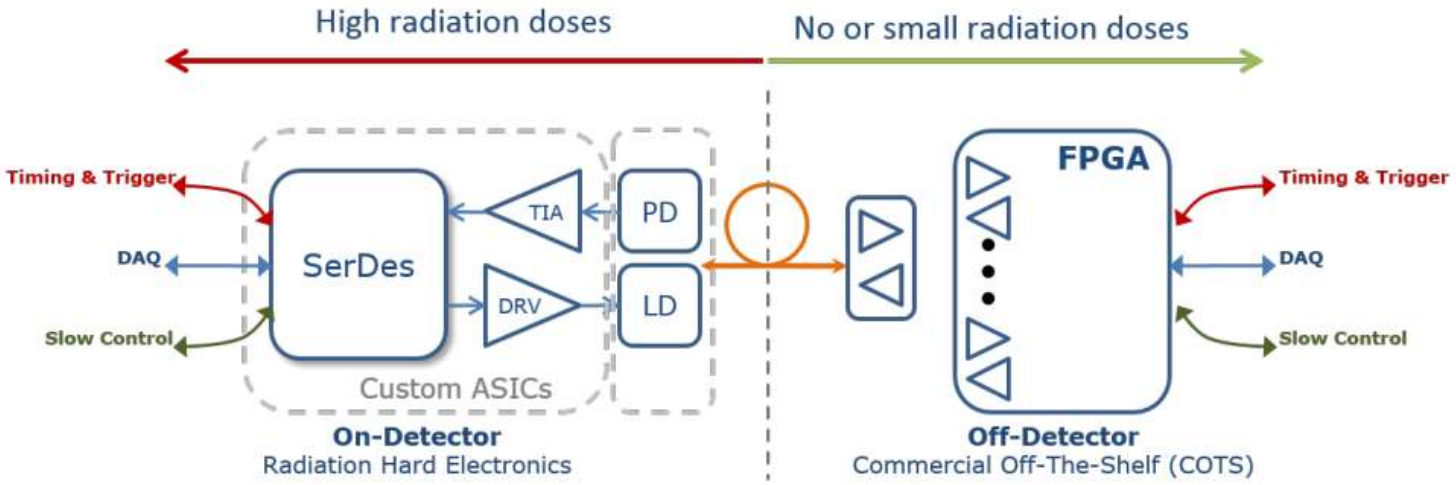
Detector area

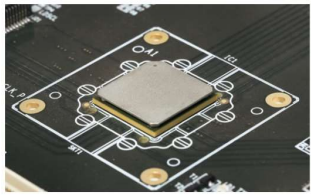
Run 1/2:
TTC link,
Ethernet,
DDL Link
(Wigner/KFKI)

Run 3:
GBT Links

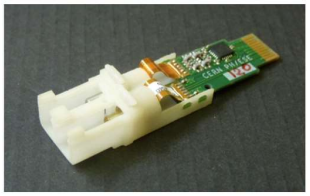
Run 3:
new
detectors
(e.g. FoCAL)
lpGBT Link

GBT/lpGBT Link Architecture





GBTx ASIC



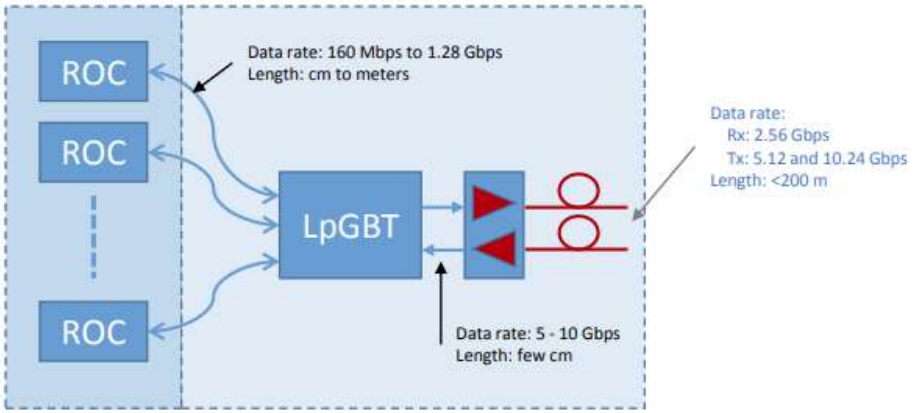
Versatile Link

PCIe40 / CRU

Ref: CERN

lpGBT ASICs Features

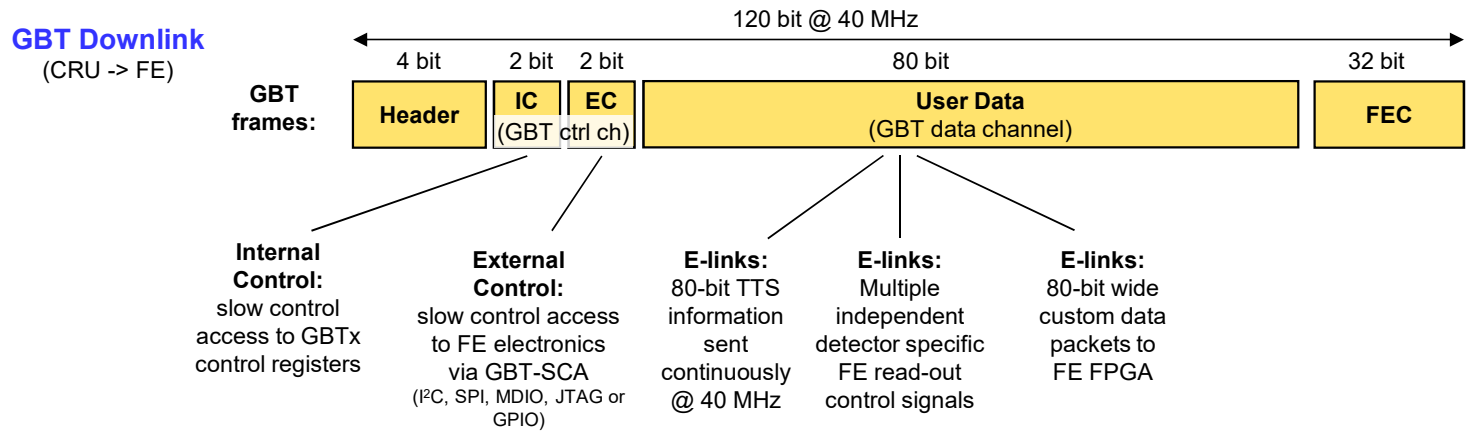
- Data transceiver with fixed and "deterministic" latency for both up and down links.
  - Clocks and Data
- Down link:
  - 2.56 Gbps
  - FEC12
  - eLinks:
    - Bandwidth: 80/160/320 Mbps
    - Count: 16/8/4
- Up link:
  - 5.12 Gbps or 10.24 Gbps
  - FEC5 or FEC12
  - eLinks:
    - Data rates: 160 /320 / 640 / 1280 Mbps
    - Count:
      - FEC5
        - Up to 28 @ 160 Mbps
        - Up to 7 @ 1.28 Gbps
      - FEC12
        - Up to 24 @ 160 Mbps
        - Up to 6 @ 1.28 Gbps

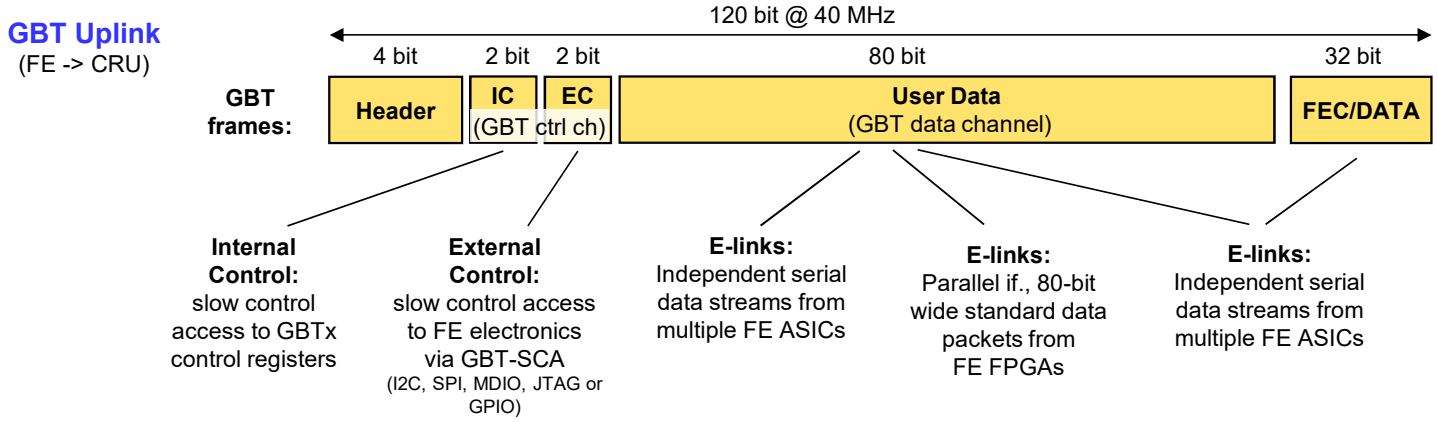


- Experiment control/monitoring functions:
  - 10-bit ADC
  - 12-bit voltage DAC
  - 8-bit current DAC
  - Temperature sensor
  - Three I2C masters
  - Programmable parallel port: 16 x GPIO
- Package:
  - 9 mm x 9 mm x 1.25 mm (pitch: 0.5 mm)
  - Pin count: 289 (17 x 17)

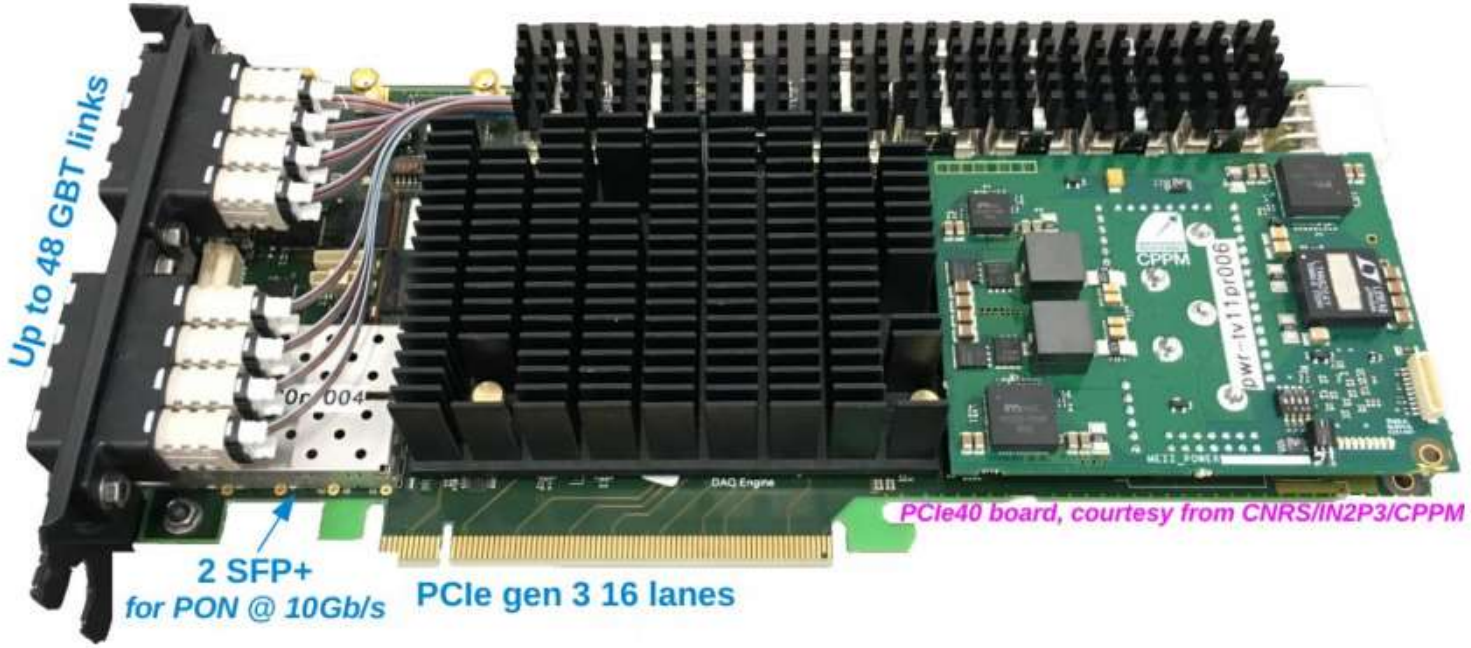
Ref: CERN

GBT Frame Structure



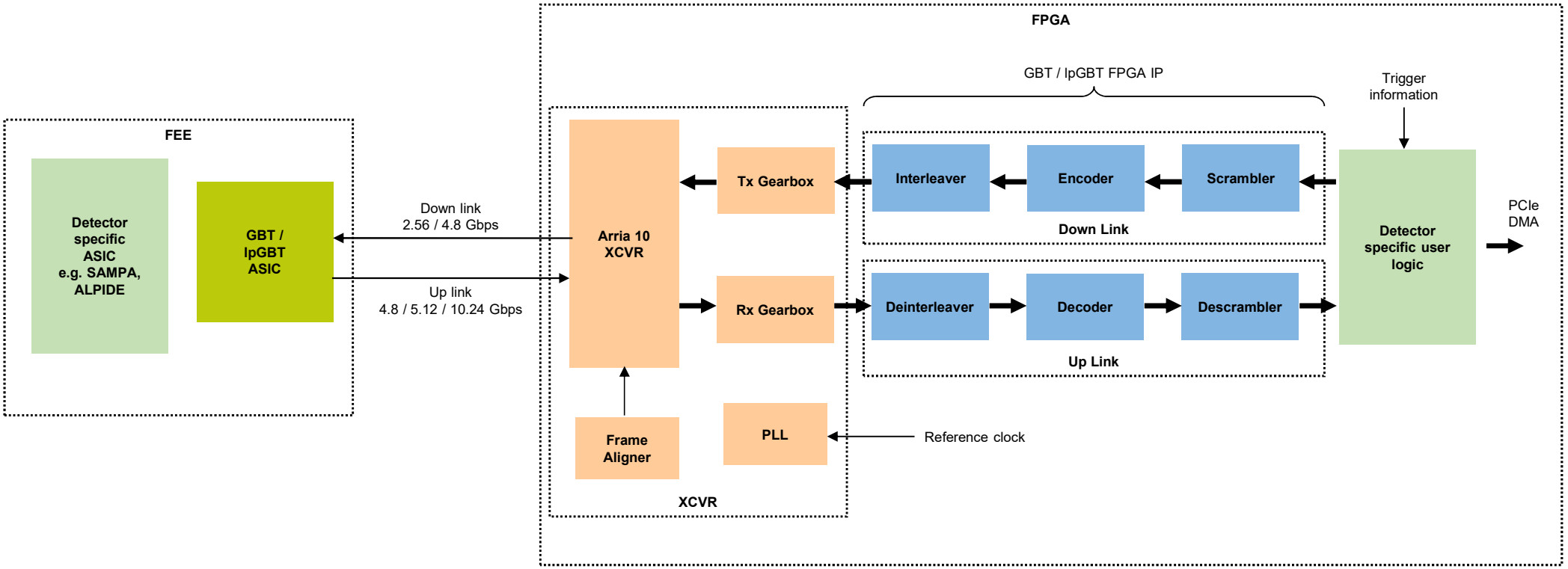


ALICE Common Readout Unit (RCU)

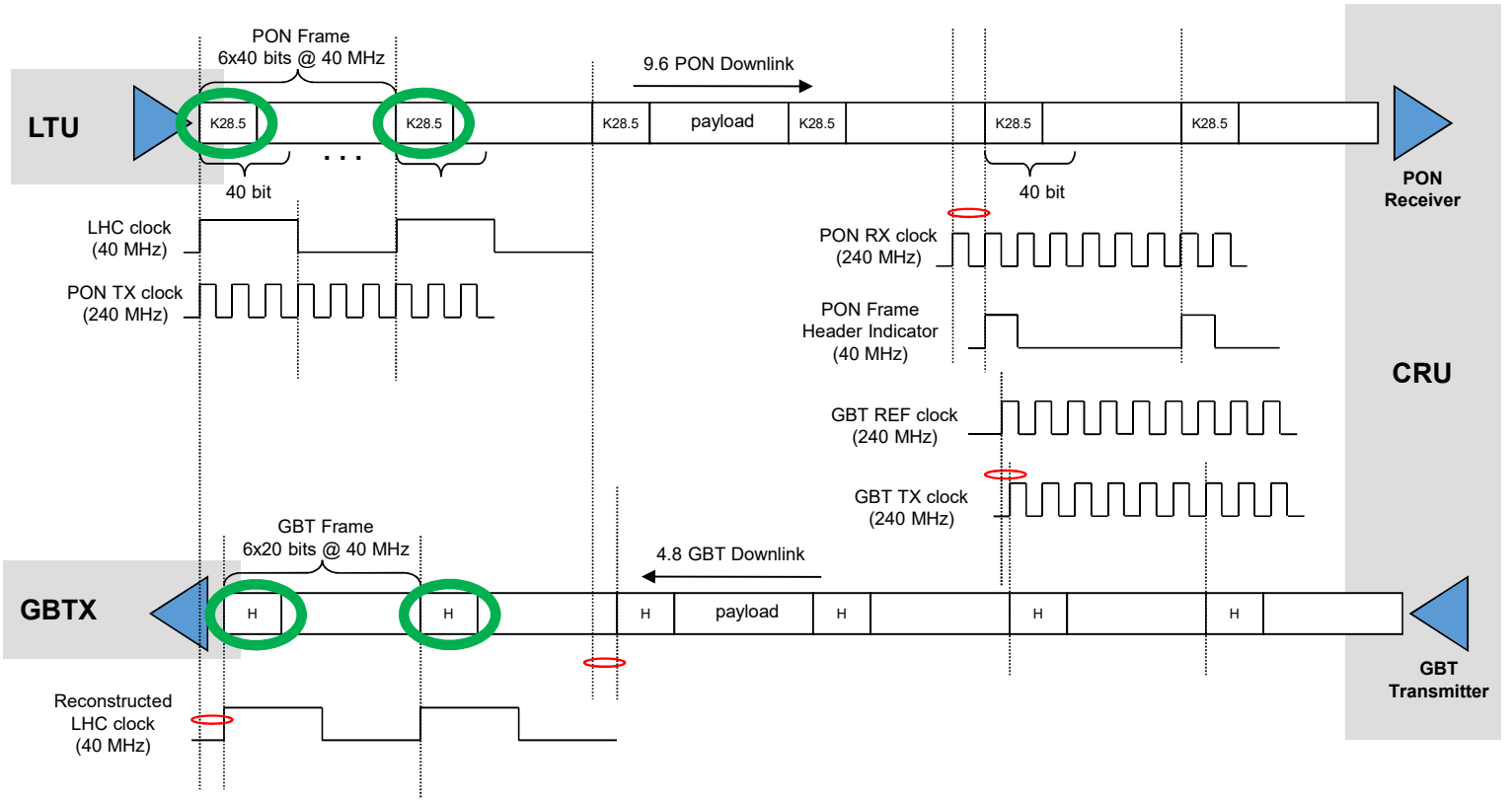


- Intel Arria 10 GX 10AX115 FPGA with 96 x 12.5 Gbps transceiver
  - x2 for trigger communication (SFP+ cage)
  - x48 for GBT / lpGBT links (4 x 12-lane Avago TX and RX MiniPODs)
  - 2 x 8 lane for PCIe Gen3

GBT/lpGBT FPGA Architecture

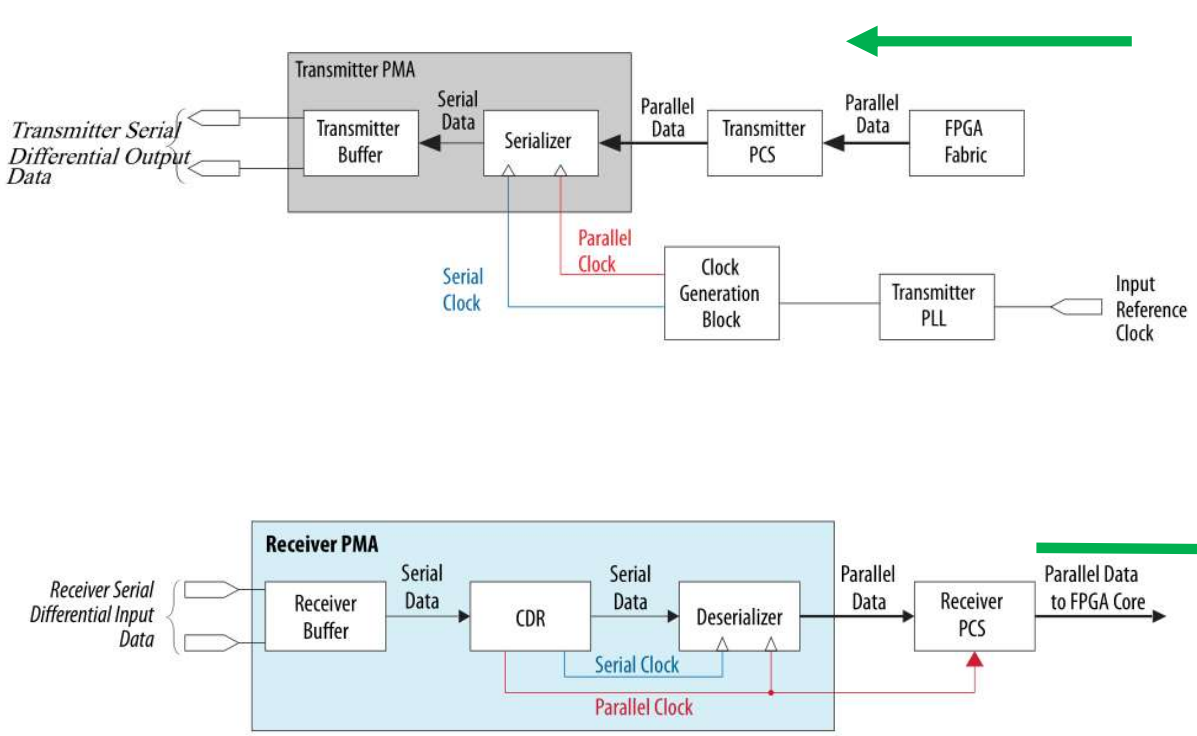


LHC Clock Distribution



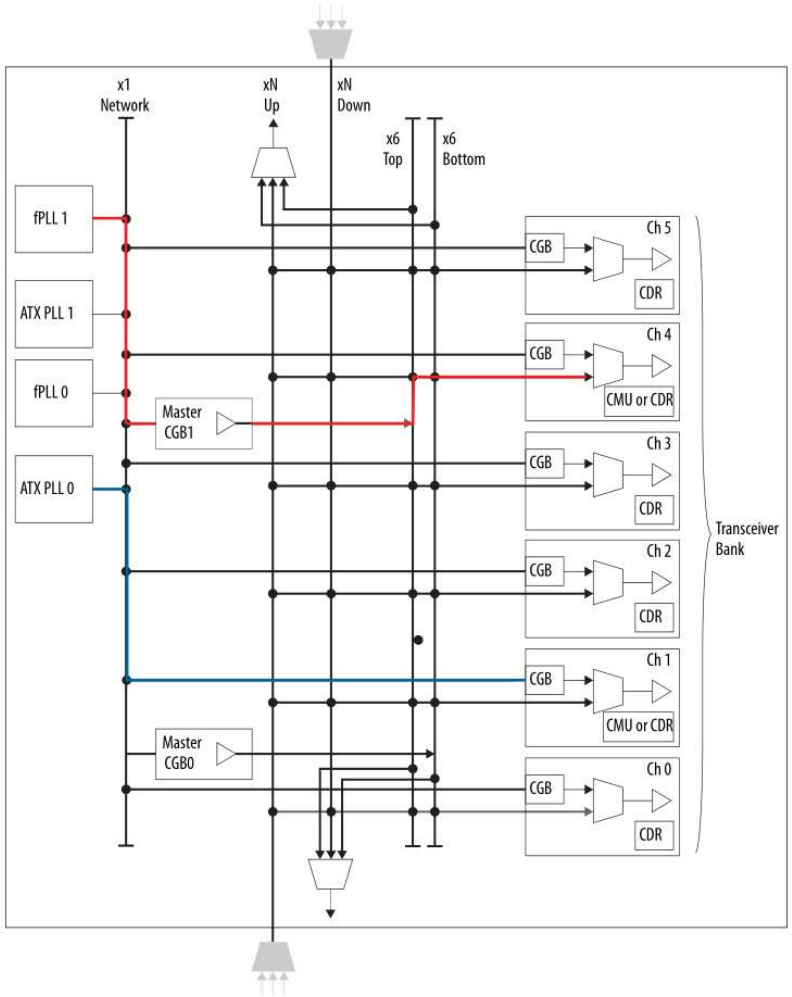
Latency must be fixed and deterministic

Arria 10 Transceiver PHY Architecture 1



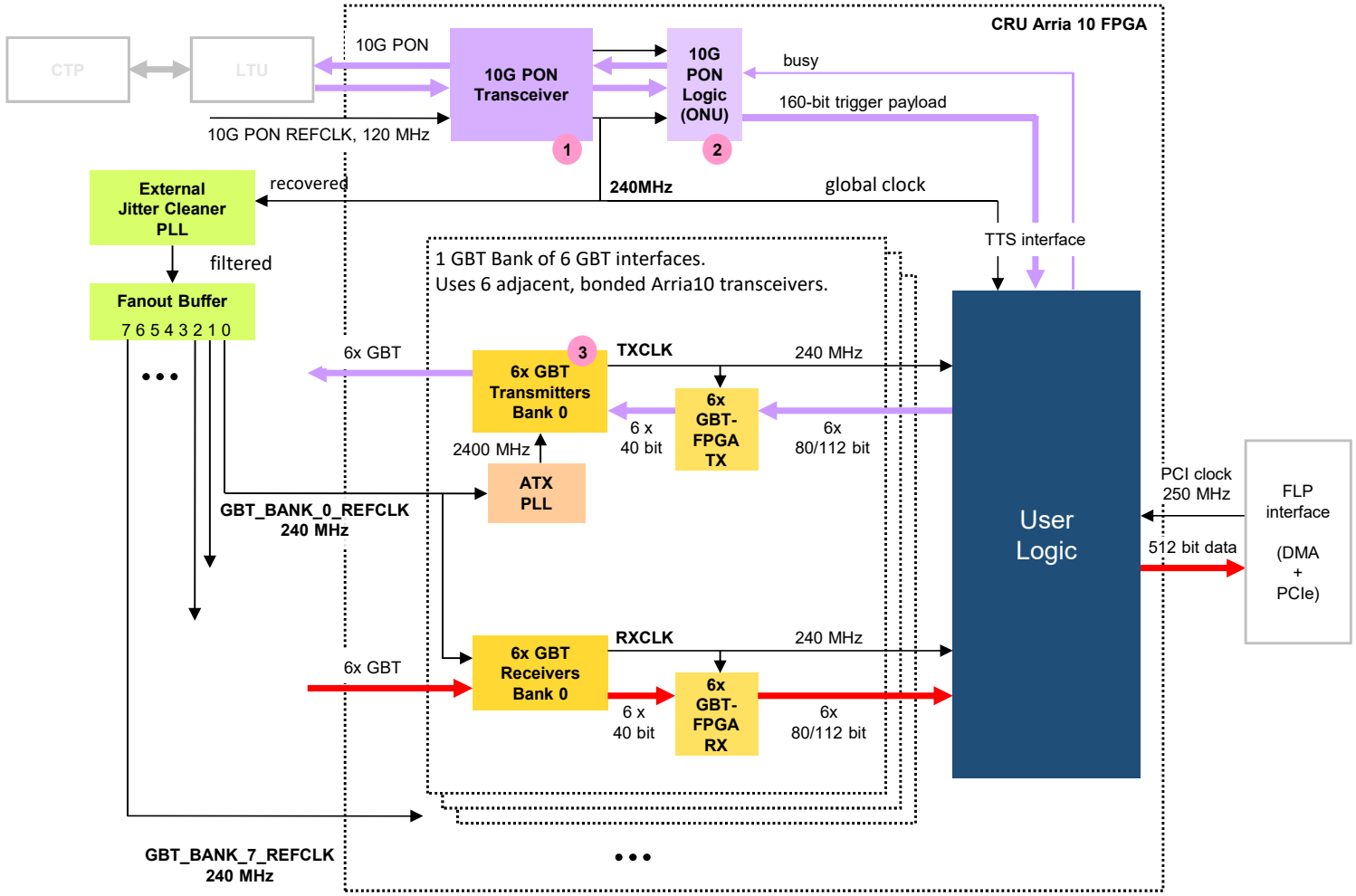
Ref: Intel

Arria 10 Transceiver PHY Architecture 2



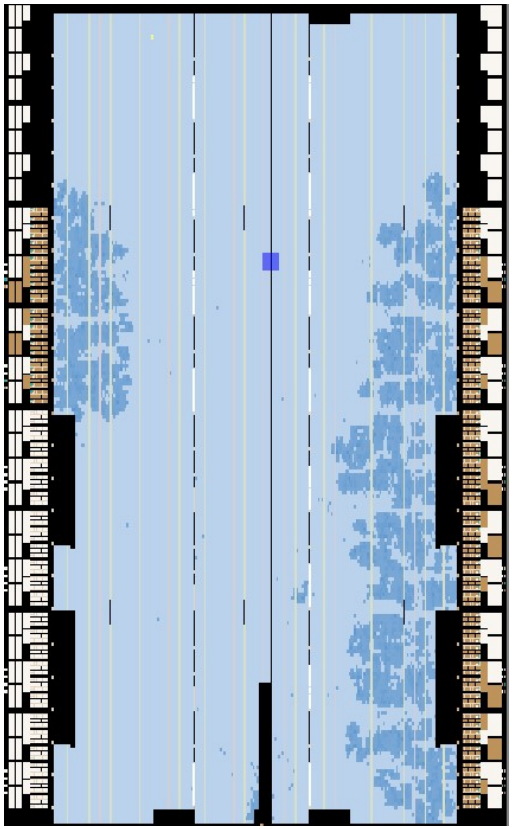
Ref: Intel

LHC Clock Recovery and Distribution



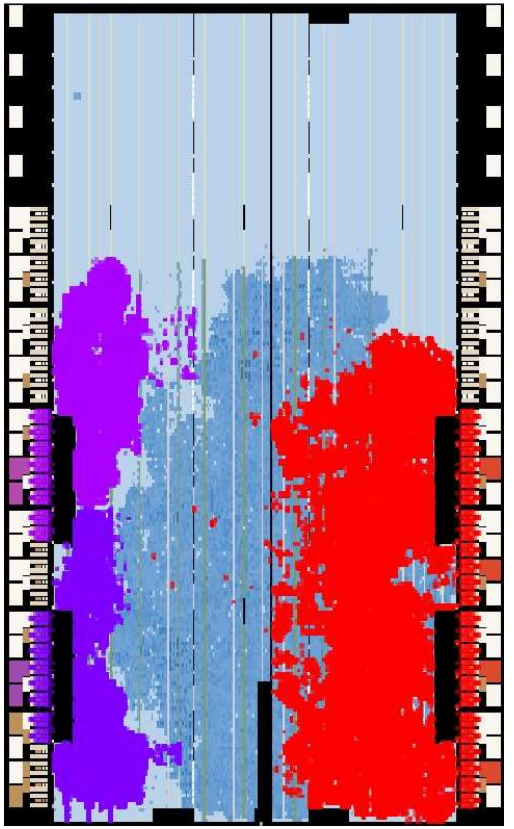
Arria 10 Quartus Chip Planner Layout

GBT x48 Link



GBT Bank 6
GBT Bank 7
GBT Bank 5 (x6 Link)
GBT Bank 4 (x6 Link)
GBT Bank 3 (x6 Link)
GBT Bank 2 (x6 Link)
GBT Bank 1 (x6 Link)
GBT Bank 0 (x6 Link)

GBT x24 Link



PCIe Gen3 x16 Lane
GBT x24 Link

Reference links

- LpGBT-FPGA
  - http://lpgbt-fpga.web.cern.ch/
- LpGBT-FPGA git repository
  - https://gitlab.cern.ch/gbt-fpga/lpgbt-fpga
- TWEPP lpGBT presentation
  - https://indico.cern.ch/event/697988/contributions/3075493/attachments/1720215/2776778/lpGBTtutorialTwepp20180921.pdf
- TWEPP CRU presentation
  - https://indico.cern.ch/event/799025/contributions/3486239/attachments/1901460/3140257/cru_twepp_2019.pdf
- Alice O2 Software
  - https://github.com/AliceO2Group
- ALICE CRU Firmware
  - https://gitlab.cern.ch/alice-cru/cru-fw (requires ALICE membership)

Thank You
For Your Attention!

Any Questions?